

### **ABSTRACT OF THE DISCLOSURE**

A clock signal SCLK is provided to an input/output interface and communication data SIN consisting of a predetermined frame including a predetermined bits with a parity bit P is transmitted to an electronic circuit at a synchronized timing with the clock signal SCLK. A parity check is performed at a synchronized timing with an output of a communication completion condition synchronized with the clock signal SCLK and the communication contents are checked by the parity bit P.

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